AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A semiconductor device having a System in Package structure in which a system comprises:

a wiring substrate;

a microcomputer chip; and

a memory chip, said microcomputer chip and said memory chip being mounted over an upper surface of said wiring substrate, and

wherein said microcomputer chip is constructed as a multiport device including an interface between said microcomputer chip and another part of said system including said memory chip and an interface between said microcomputer chip and outside of said system,

wherein said memory chip is constructed to be accessed from the outside of said system via said microcomputer chip,

wherein said microcomputer chip has a substantially square planar shape,

wherein said memory chip has a substantially rectangular planar shape with a long side having a greater length than a second side thereof adjacent to the long side,

wherein a length of a side of said microcomputer chip is shorter than a length of the long side of said memory chip,

wherein said microcomputer chip is mounted over said wiring substrate in a state being stacked over said memory chip such that said microcomputer chip covers a portion of the long side of said memory chip and covers no portion of the second side of said memory chip,

wherein said microcomputer chip includes a first plurality of bonding terminals on an upper surface thereof, and said memory chip includes a second plurality of bonding terminals on an upper surface thereof,

wherein said bonding terminals of said memory chip are disposed along the second side of said memory chip, and said bonding terminals of said microcomputer chip are disposed along a side of said microcomputer chip adjacent to said second side of said memory chip.

2. (Previously Presented) The semiconductor device according to claim 1, wherein said bonding terminals of said microcomputer chip are connected to first electrodes of said wiring substrate via a plurality of bonding wires, said bonding terminals of said memory chip are connected to second electrodes of said wiring substrate via a plurality

of bonding wires, and said first electrodes are arranged toward an outer periphery of said wiring substrate from said second electrodes.

3. (Previously Presented) The semiconductor device according to claim 1, wherein said memory chip includes a DRAM or a flash memory.

4-5. (Canceled)

6. (Previously Presented) A semiconductor device having a System in Package structure in which a system comprises:

a wiring substrate;

a microcomputer chip; and

two memory chips, said microcomputer and said memory chips being mounted over an upper surface of said wiring substrate, and

wherein said microcomputer chip is constructed as a multiport device including an interface between said microcomputer chip and another part of said system including said two memory chips and an interface between said microcomputer chip and outside of said system,

wherein each of said two memory chips is constructed to be accessed from the outside of said system via said microcomputer chip,

wherein said microcomputer chip has a substantially square planar shape,

wherein each of said two memory chips has a substantially rectangular planar shape with a long side having a greater length than a second side thereof adjacent to the long side,

wherein a length of a side of said microcomputer chip is shorter than a length of the long side of each of said two memory chips,

wherein said two memory chips are mounted over said wiring substrate in a state in which one of said memory chips is stacked over the other, and said microcomputer chip is mounted over said wiring substrate in a state of being stacked over said two memory chips such that said microcomputer chip covers portions of said long sides of said memory chips and covers no portions of the second sides of said memory chips,

wherein said microcomputer chip includes a plurality of bonding terminals on an upper surface thereof, and at least one of said memory chips includes a respective plurality of bonding terminals on an upper surface thereof,

wherein said bonding terminals of said one memory chip are disposed along the second side thereof, and said bonding terminals of said microcomputer chip are disposed along a side of said microcomputer chip adjacent to said second side of said one memory chip.

7. (Previously Presented) The semiconductor device according to claim 6, wherein said one memory chip is an upper memory chip of said two memory chips, said bonding terminals of said microcomputer chip are connected to first electrodes of said wiring substrate via a plurality of bonding wires, a lower memory chip of said two memory chips is connected to second electrodes of said wiring substrate via a plurality of bump electrodes, said bonding terminals of said upper memory chip are connected to third electrodes of said wiring substrate via a plurality of bonding wires, and said first electrodes are arranged toward an outer periphery of said wiring substrate from said second and third electrodes.

8. (Previously Presented) The semiconductor device according to claim 6, wherein one of said two memory chips includes a DRAM, and the other includes a flash memory.

9. (Previously Presented) The semiconductor device according to claim 6, wherein a lower surface of said wiring substrate is formed with a plurality of bump electrodes constructing external connection terminals.

10. (Previously Presented) The semiconductor device according to claim 1, wherein a total number of bonding terminals on the upper surface of said microcomputer chip is much greater than a total number of bonding terminals on the upper surface of said memory chip.

11. (Previously Presented) The semiconductor device according to claim 10, wherein the upper surface of said microcomputer chip has no bonding terminals superposed over bonding terminals on the upper surface of said memory chip in a plan view.

12. (Previously Presented) The semiconductor device according to claim 7, wherein an under-fill resin is filled in a gap between said lower memory chip and said wiring substrate.

13. (Previously Presented) The semiconductor device according to claim 6, wherein said two memory chips are

arranged such that the long side of one of said memory chips crosses the long side of the other.

14. (New) A semiconductor device comprising:

a wiring substrate having an upper surface, a plurality of first electrodes formed on the upper surface, a plurality of second electrodes formed on the upper surface, and a lower surface opposite the upper surface;

a memory chip having a first main surface, the first main surface having a substantially rectangular shape with two long sides having a greater length than two short sides, a respective plurality of first bonding terminals disposed on the first main surface along each of the two short sides, and a first back surface opposite the first main surface;

a microcomputer chip having a second main surface, the second main surface having a substantially square shape with four sides, a respective plurality of second bonding terminals disposed on the second main surface along each of the four sides, and a second back surface opposite the second main surface;

a respective plurality of first wires connecting each plurality of first bonding terminals with a corresponding group of the first electrodes, respectively; and

a respective plurality of second wires connecting each plurality of second bonding terminals with a corresponding group of the second electrodes, respectively;

wherein the second electrodes are arranged closer to an outer periphery of the wiring substrate than the first electrodes;

wherein the memory chip is mounted over the upper surface of the wiring substrate, inwardly from the first electrodes, with the first back surface facing the upper surface of the wiring substrate;

wherein the microcomputer chip is mounted over the first main surface of the memory chip with the second back surface facing the first main surface of the memory chip;

wherein the second bonding terminals include an external interface terminal electrically connected outside of a system comprising the memory chip and the microcomputer chip, and an internal interface terminal electrically connected with the memory chip;

wherein the total number of second bonding terminals is substantially greater than that of the first bonding terminals; and

wherein a length of each of the four sides of the microcomputer chip is greater than that of each of the two short sides of the memory chip and shorter than that of each

of the two long sides of the memory chip, such that the mounted microcomputer chip covers a portion of each of the two long sides of the memory chip and covers no portion of the first bonding terminals of the memory chip.

15. (New) The semiconductor device according to claim 14, wherein two opposing sides of the four sides of the microcomputer chip are adjacent to the two long sides of the memory chip, respectively, and the two opposing sides of the microcomputer chip extend substantially equally beyond the two long sides of the memory chip, respectively.

16. (New) The semiconductor device according to claim 14, wherein the microcomputer chip, the memory chip, the upper surface of the wiring substrate, the first wires and the second wires are sealed with a mold resin.

17. (New) The semiconductor device according to claim 14, wherein the memory chip has a function of an SRAM, a DRAM or a flash memory.

18. (New) The semiconductor device according to claim 14, wherein the device includes a plurality of solder bumps connected to the lower surface of the wiring substrate, and

wherein data, which is output through said external interface terminal of the microcomputer chip, is transmitted outside of the system through at least one solder bump.

19. (New) The semiconductor device according to claim 14, wherein an additional semiconductor chip is mounted over the upper surface of the wiring substrate, and the memory chip is stacked over the additional semiconductor chip.

20. (New) The semiconductor device according to claim 19, wherein an under-fill resin is filled in a gap between the additional semiconductor chip and the wiring substrate.